WHAT IS CLAIMED IS:

1. A structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising:

   a first plurality of vias;

   a second plurality of vias, wherein the first and second pluralities of vias are vertically overlapping;

   a first routing level at a first height, said first level connected to the first plurality of vias; and

   a second routing level at a second height, said second level connected to the second plurality of vias, wherein the first height is different from the second height,

   wherein both routing levels are formed above the substrate, and

   wherein a) the first routing level and the second routing level are above the first and second vias or

   b) the first routing level and the second routing level are below the first and second vias.

2. The structure of claim 1 wherein the first and second vias are evenly spaced and have a common first pitch.

3. The structure of claim 2 wherein the first routing level has a second pitch and the second routing level has a third pitch, the first pitch smaller than the second pitch and the third pitch.

4. The structure of claim 1 further comprising a third routing level, the third routing level either a) below the first and second vias or b) above the first and second vias, vertically opposite the first and second routing levels.

5. The structure of claim 4 wherein the third routing level is above the first vias and the second vias.

6. The structure of claim 4 wherein the third routing level comprises memory lines in a memory array.

7. The structure of claim 6 wherein memory cells accessed by the memory lines are charge storage memory cells.

8. The structure of claim 7 wherein the memory cells are SONOS devices.

9. The structure of claim 7 wherein the memory cells are floating gate devices.

10. The structure of claim 7 wherein the memory cells are arranged in a NAND string.

11. The structure of claim 6 wherein memory cells accessed by the memory lines are passive element memory cells.

12. The structure of claim 11 wherein at least one passive element memory cell comprises an antifuse.

13. The structure of claim 11 wherein at least one passive element memory cell comprises a fuse.

14. The structure of claim 6 wherein the memory array is a monolithic three dimensional memory array.

15. The structure of claim 5 wherein the memory lines have a fourth pitch smaller than the first pitch.

16. The structure of claim 4 wherein the third routing level is below the first vias and the second vias.

17. The structure of claim 16 wherein the integrated circuit comprises a memory array.

18. The structure of claim 17 wherein the third routing level comprises memory lines.

19. The structure of claim 18 wherein the first routing level has a second pitch, the second routing level has a third pitch, the first pitch smaller than the second pitch and the third pitch.

20. The structure of claim 19 wherein memory cells accessed by the memory lines are charge storage memory cells.

21. The structure of claim 20 wherein the memory cells are SONOS devices.

22. The structure of claim 20 wherein the memory cells are floating gate devices.

23. The structure of claim 20 wherein the memory cells are arranged in a NAND string.

24. The structure of claim 19 wherein memory cells accessed by the memory lines are passive element memory cells.

25. The structure of claim 24 wherein at least one passive element memory cell comprises an antifuse.

26. The structure of claim 24 wherein at least one passive element memory cell comprises a fuse.

27. The structure of claim 6 wherein the array is a monolithic three dimensional memory array comprising at least first and second memory levels, the second memory level formed vertically above the first memory level.

28. The structure of claim 4 wherein the third routing level has a fourth pitch substantially less than the first pitch.

29. The structure of claim 28 wherein the fourth pitch is substantially one half the first pitch.

30. A structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising:

a first plurality of vias;

a second plurality of vias, wherein the first and second pluralities of vias are vertically overlapping;

a first routing level at a first height, said first level connected to the first plurality of vias;

a second routing level at a second height, said second level connected to the second plurality of vias, wherein the first height is different from the second height; and

a third routing level at a third height, the third level connected to the first plurality of vias and to the second plurality of vias, wherein all three routing levels are formed above the substrate.

31. The structure of claim 30 wherein the first and second vias are evenly spaced and have a first pitch.

32. The structure of claim 31, wherein the third routing level is above the first routing level and the second routing level.

33. The structure of claim 32 wherein the third routing level comprises memory lines in a memory array.

34. The structure of claim 33 wherein the first routing level has a second pitch, the second routing level has a third pitch, the first pitch smaller than the second pitch and the third pitch.

35. The structure of claim 34 wherein memory cells accessed by the memory lines are charge storage memory cells.

36. The structure of claim 35 wherein the memory cells are SONOS devices.

37. The structure of claim 35 wherein the memory cells are floating gate devices.

38. The structure of claim 35 wherein the memory cells are arranged in a NAND string.

39. The structure of claim 34 wherein memory cells accessed by the memory lines are passive element memory cells.

40. The structure of claim 39 wherein at least one passive element memory cell comprises an antifuse.

41. The structure of claim 39 wherein at least one passive element memory cell comprises a fuse.

42. The structure of claim 33 wherein the memory array is a monolithic three dimensional memory array.

43. The structure of claim 33 wherein the memory lines have a fourth pitch smaller than the first pitch.

44. The structure of claim 31 wherein the third routing level is below the first routing level and the second routing level.

45. The structure of claim 44 wherein the integrated circuit comprises a memory array.

46. The structure of claim 45 wherein the third routing level comprises memory lines.

47. The structure of claim 46 wherein the first routing level has a second pitch, the second routing level has a third pitch, the first pitch smaller than the second pitch and the third pitch.

48. The structure of claim 47 wherein memory cells accessed by the memory lines are charge storage memory cells.

49. The structure of claim 48 wherein the memory cells are SONOS devices.

50. The structure of claim 48 wherein the memory cells are floating gate devices.

51. The structure of claim 48 wherein the memory cells are arranged in a NAND string.

52. The structure of claim 47 wherein memory cells accessed by the memory lines are passive element memory cells.

53. The structure of claim 52 wherein at least one passive element memory cell comprises an antifuse.

54. The structure of claim 52 wherein at least one passive element memory cell comprises a fuse.

55. The structure of claim 31, wherein the array is a monolithic three dimensional memory array comprising at least first and second memory levels, the second memory level formed vertically above the first memory level.

56. A structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising:

a first plurality of vias;

a second plurality of vias;

a first routing level at a first height, said first level connected to the first plurality of vias;

a second routing level at a second height, said second level connected to the second plurality of vias, wherein the first height is different from the second height; and

a third routing level at a third height, the third level connected to the first plurality of vias and to the second plurality of vias, wherein all three routing levels are formed above the substrate, and wherein either

the third routing level is above both the first and the second routing levels,

or

the third routing level is below both the first and the second routing levels.

57. The structure of claim 56 wherein the first and second vias are evenly spaced and have a first pitch.

58. The structure of claim 57, wherein the third routing level is above the first routing level and the second routing level.

59. The structure of claim 58 wherein the third routing level comprises memory lines in a memory array.

60. The structure of claim 59 wherein the first routing level has a second pitch, the second routing level has a third pitch, the first pitch smaller than the second pitch and the third pitch.

61. The structure of claim 60 wherein memory cells accessed by the memory lines are charge storage memory cells.

62. The structure of claim 61 wherein the memory cells are SONOS devices.

63. The structure of claim 61 wherein the memory cells are floating gate devices.

64. The structure of claim 61 wherein the memory cells are arranged in a NAND string.

65. The structure of claim 60 wherein memory cells accessed by the memory lines are passive element memory cells.

66. The structure of claim 65 wherein at least one passive element memory cell comprises an antifuse.

67. The structure of claim 65 wherein at least one passive element memory cell comprises a fuse.

68. The structure of claim 59 wherein the memory array is a monolithic three dimensional memory array.

69. The structure of claim 59 wherein the memory lines have a fourth pitch smaller than the first pitch.

70. The structure of claim 57 wherein the third routing level is below the first routing level and the second routing level.

71. The structure of claim 70 wherein the array is a memory array.

72. The structure of claim 71 wherein the third routing level comprises memory lines.

73. The structure of claim 57, wherein the array is a monolithic three dimensional memory array comprising at least first and second memory levels, the second memory level formed vertically above the first memory level.

74. A method for forming a via and routing structure for electrically connecting a multilevel array in an integrated circuit, the method comprising:

forming a first routing level;

forming a second routing level above the first routing level;

forming a first plurality of vias connected at bottom ends to the first routing level;

forming a second plurality of vias connected at bottom ends to the second routing level, wherein the first and second pluralities of vias are vertically overlapping.

75. The method of claim 74 wherein

the step of forming the first plurality of vias comprises etching first via holes and filling the first via holes;

the step of forming the second plurality of vias comprises etching second via holes and filling the second via holes; and

portions of the first via holes and portions of the second via holes are etched in the same etch process.

76. The method of claim 74 wherein

the step of forming the first plurality of vias comprises etching first via holes and filling the first via holes;

the step of forming the second plurality of vias comprises etching second via holes and filling the second via holes; and

the first via holes and the second via holes are etched in the same etch process.

77. The method of claim 74 wherein

the step of forming the first plurality of vias comprises etching first via holes and filling the first via holes;

the step of forming the second plurality of vias comprises etching second via holes and filling the second via holes; and

the first via holes and the second via holes are etched in separate etch processes.

78. The method of claim 74 wherein

the step of forming the first plurality of vias comprises etching first via holes and filling the first via holes;

the step of forming the second plurality of vias comprises etching second via holes and filling the second via holes; and

the first via holes and the second via holes are filled at substantially the same time.

79. The method of claim 74 wherein

the step of forming the first plurality of vias comprises etching first via holes and filling the first via holes;

the step of forming the second plurality of vias comprises etching second via holes and filling the second via holes; and

portions of the first via holes and portions of the second via holes are filled at substantially the same time.

80. The method of claim 74 wherein

the step of forming the first plurality of vias comprises etching first via holes and filling the first via holes;

the step of forming the second plurality of vias comprises etching second via holes and filling the second via holes; and

the first via holes and the second via holes are filled at different times.

81. The method of claim 74 wherein the multilevel array comprises a row of vias having a first pitch, the row of vias comprising the first plurality of vias and the second plurality of vias, vias of the first and second pluralities interspersed.

82. The method of claim 81 further comprising forming a third routing level above the first and second routing levels, wherein

said third routing level connects to top ends of the first plurality of vias or

said third routing level connects to top ends of the second plurality of vias.

83. The method of claim 82 wherein the third routing level comprises memory lines in a memory array.

84. The method of claim 83 wherein the first routing level has a second pitch larger than the first pitch.

85. The method of claim 84 wherein the memory lines have a third pitch smaller than the first pitch.

86. The method of claim 83 wherein memory cells accessed by the memory lines are charge storage memory cells.

87. The method of claim 86 wherein the memory cells are SONOS devices.

88. The method of claim 86 wherein the memory cells are floating gate devices.

89. The method of claim 86 wherein the memory cells are arranged in a NAND string.

90. The method of claim 83 wherein the memory array is a monolithic three dimensional memory array.

91. The method of claim 83 wherein memory cells accessed by the memory lines are passive element memory cells.

92. The method of claim 91 wherein at least one passive element memory cell comprises an antifuse.

93. The method of claim 91 wherein at least one passive element memory cell comprises a fuse.

94. The method of claim 74 wherein said third routing level connects to top ends of the first plurality of vias and said third routing level connects to top ends of the second plurality of vias.